1. Admissions/ Management Information

Title of the programme – including any lower awards
Please provide the titles used for all awards relating to this programme. Note: all programmes are required to have at least a Postgraduate Certificate exit award.

See guidance on programme titles in:

Masters	MSc Digital Systems Engineering		
Postgraduate Diploma	PGDip Digital Systems Engineering	Please indicate if the Postgraduate Diploma is available as an entry point, ie. is a programme on which a student can register, is an exit award, ie. is only available to students exiting the masters programme early, or both.	Exit
Postgraduate Certificate	PGCert Digital Systems Engineering	Please indicate if the Postgraduate Certificate is available as an entry points, ie. is a programme on which a student can register, is an exit award, ie. is only available to students exiting the masters programme early, or both.	Exit
Level of qualification	Level 7		

This document applies to students who commenced the programme(s) in:	2019

Awarding institution	**Teaching institution**
Unviersity of York	University of York

Department(s): Where more than one department is involved, indicate the lead department		**Board of Studies**
Lead Department	Department of Electronic Engineering	Department of Electronic Engineering
Other contributing Departments:		

Route code (existing programmes only)	PMDIGSSYE1

Admissions criteria

Applicants are normally expected to hold (or expected to gain) the equivalent of a 2:1 honours degree or above from a university recognised by the University of York. This degree should have a significant electronics and/or computing content. We are willing to consider
applications from students with lower qualifications, particularly when the student has high marks in relevant modules and/or appropriate industrial experience.
For applicants whose native language is not English, the minimum University English language requirements of IELTS 6.0 (with at least 5.5 in each of the four language components) or the equivalent are required.

Length and status of the programme(s) and mode(s) of study

Programme	**Length (years/ months)**	**Status (full-time/ part-time)** Please select	**Start dates/months** (if applicable – for programmes that have multiple intakes or start dates that differ from the usual academic year)	**Mode**		
				Face-to-face, campus-based	**Distance learning**	**Other**

MSc in Digital Systems Engineering	1 year	Full-time	September	Please select Y/N	Yes	Please select Y/N	No	N/A

Language(s) of study

English

Language(s) of assessment

English

2. Programme accreditation by Professional, Statutory or Regulatory Bodies (PSRB)

2.a. Is the programme recognised or accredited by a PSRB

Please Select Y/N:	Yes	if No move to section 3 if Yes complete the following questions

2.b. Name of PSRB

IET (Institute of Engineering and Technology)

2.c. Please provide details of any approval/ accrediation event needed, including: timecales, the nature of the event, central support / information required:

Department Reapproval for IET accreditation takes place in 2019-20.

2.d. Are there any conditions on the approval/ accreditation of the programme(s)/ graduates (for example accreditation only for the full award and not any interim award)

Although the university allows 40 credits of compensation, for the degree to remain IET-accredited, students can only be compensated in 30 credits. If a student has over 30 credits of compensation but has met the university progression requirements of 40 credits of compensation, they may be given the opportunity to resit compensated modules in order to reduce the compensation to 30 credits and remain on an accredited degree.
Students who do not meet the IET criteria for accreditation will graduate with:
MSc Electronics (for students on MSc Embedded Wireless Systems, MSc Digital Systems Engineering)

3. Additional Professional or Vocational Standards

Are there any additional requirements of accrediting bodies or PSRB or pre-requisite professional experience needed to study this programme?

Please Select Y/N:	No	if Yes, provide details

4. Programme leadership and programme team

4.a. Please name the programme leader for the year to which the programme design applies and any key members of staff responsible for designing, maintaining and overseeing the programme.

Dr Ruwan Gajaweera

5. Purpose and learning outcomes of the programme

5.a. Statement of purpose for applicants to the Masters programme
Please express succinctly the overall aims of the programme as an applicant facing statement for a prospectus or website. This should clarify to a prospective masters student why they should choose this programme, what it will provide to them and what benefits they will gain from completing it.

The development of digital technology over the past 50 years has revolutionised the design and performance of everything from mobile phones to cars and entertainment systems; and engineers continue to enhance the performance of these devices. Recent developments in nanotechnology promise further large increases in processing power with lower power requirements, and will open up a whole new world of applications for digital techniques. This IET accredited taught programme aims to develop academic and professional excellence both for newly qualified and practicing engineers who wish to extend their professional expertise in digital systems design. It uses FPGAs as a hardware platform and HDL as a design language.The MSc in Digital Systems Engineering at York will provide you with advanced knowledge and transferable skills in the design, modelling, implementation and evaluation of state-of-the-art digital systems, enabling you to contribute effectively to the increasingly complex and rapidly evolving technologies that are prevalent in industry and research.

You will be able to learn new techniques to keep up-to-date with developments in an industrial and/or research setting, and will have hands-on experience of the different stages of the design of a modern digital system, culminating in the construction of a complex device in a group project. The MSc is taught by academics from York's world-leading Intelligent Systems and Nano-Science Research Group that specialises in the application of biological techniques to complex digital systems, and makes full use of the industry-standard FPGA design and development facilities within the Department of Electronic Engineering. After having successfully completing the MSc in Digital Systems Engineering, you will have a solid knowledge of, and developed skills, in the theory, design and implementation of digital systems. This knowledge and related skills will provide you with appropriate grounding for a range of careers in the digital and computing industry and/or research.

5.b.i. Programme Learning Outcomes - Masters

PLO	On successful completion of the programme, graduates will be able to:
1	**Subject Knowledge:** Conduct research and development in applied electronic engineering and computing to advance the state of knowledge in digital system design methodologies, algorithms, devices and tools.
2	**Engineering Analysis:** Extract and critically evaluate literature and other data about complex systems through analytical and computational methods and modelling.
3	**Engineering Design:** Create innovative and optimised designs to address real-world problems involving reconfigurable hardware and software systems by synthesising novel research-based ideas into engineering specifications.
4	**Practical Skills:** Apply professional skills of programming, CAD, construction and measurement, test and verification, combined with an understanding of engineering systems and components, to independently solve complex and technically challenging research-based problems.
5	**Technical Communication:** Debate, defend and contextualise information in a succinct and technically accurate manner for engineers and non-technical audiences, and to write and interpret technical documentation.
6	**Management & Personal Development:** Proficiently manage themselves, teams and complex projects in preparation for technical careers as leaders in applied electronic engineering.

5.c. Explanation of the choice of Programme Learning Outcomes

Please explain your rationale for choosing these PLOs in a statement that can be used for students (such as in a student handbook). Please include brief reference to:

i) ... in what way will these PLOs result in an ambitious, challenging programme which stretches the students?

The PLOs for this programme have been developed by the programme team as the best way of capturing the skills and competencies that graduates of the programme will be able to demonstrate. PLO1 indicates that the specialist digital systems engineering knowledge gained will be actively applied in individual research, working at the cutting edge of applied electronics research. PLOs 2-4 represent the main skillset that engineers are expected to have - that of analysing complex problems in today's world, designing innovative solutions, and having the practical technical ability to bring novel ideas into being. This programme specifically develops an engineering skillset that is applicable in the world of electronics and devices. PLO5 emphasises the importance of an engineer being able to communicate their questions, analysis, findings and solutions to a variety of audiences via a variety of media. PLO6 crystalises the need in the modern world for engineers to be effective team-players, adaptable to working alone or in different sized teams for a variety of different purposes. Together these PLOs bring together up-to-date knowledge, cutting-edge engineering skills, with the abiility to work effectively with others and communicate with the wider world.

ii) ... in what way will these PLOs produce a programme which is distinctive and advantageous to the student?

York has been developing programmes in this area for many years and staff have a wide range of experience in the core subject knowledge, working on related research projects, and guiding students through the process of learning and practically experiencing the subject. The PLOs form a series of learning ladders that ensure that the different strands of learning receive full coverage across the programme. Whilst students need to learn a good deal of information about their subject, the job of a university in today's knowledge-rich world, is to provide context, guidance and experience of applying that knowledge in practice. For this programme in Digital Systems Engineering, students will gain knowledge, experience and confidence in a combination of areas that are of direct applicability to today's major research topics in digital system design methodologies, algorithms, devices and tools.

iii) ... how the design of the programme enables students from diverse entry routes to transition successfully into the programme? For example, how does the organisation of the programme ensure solid foundations in disciplinary knowledge and understanding of conventions, language skills, mathematics and statistics skills, writing skills, lab skills, academic integrity

Prior to arrival: Students receive newsletters with information about the programme. Example lecture notes are provided so that students can begin to prepare for the expected level of teaching and technical content.
Upon arrival: 3 afternoon intensive induction specifically designed to introduce students to the way we do things here at York, to level the understanding playing field; to give students the chance to get to know each other and work together in groups; to lay down a foundation of generic skills training and UK conventions, especially in teaching and learning; to get them started in writing and speaking skills, working in teams, some tools for creative problem solving, thinking, etc. We generally mix students in supervision groups by gender and country of origin - with the intention of helping them integrate.
During the year: A specially developed module in C Programming provides workshops to help people with limited experience of engineering coding to make rapid progress. Each module is designed to introduce key topic material, but also to allow students to apply this in practice in labs, tutorials, and via supported self-study.

iv) ... how the programme is designed to enable students to progress successfully - in a limited time frame - through to the end of the award? For example, the development of higher level research skills; enabling students to complete an independent study module; developing competence and confidence in practical skills/ professional skills. See QAA masters characteristics doument http://www.qaa.ac.uk/en/Publications/Documents/Masters-Degree-Characteristics-15.pdf

In the Autumn term, a module on 'C Programming for MSc' hones the students' skills required to effectively develop software components, by providing a practical introduction to writing and running C programs as an example of a procedural programming language. Then the Spring term module 'Systems Programming for Embedded Devices' extends the programming skills to develop complex and advanced software components and the use of real-time operating systems for embedded systems.
The Autumn term modules Digital Design and IC design and Simulation introduce students to VHDL as a hardware description language and build up students' knowledge in digital design methodologies and the impact of gate-level building blocks on a system-level design. Now equipped with the fundamentals, in the Spring term module 'Digital Engineering for MSc' students will learn advanced digital design techniques for performance improvement and test and verification methodologies used in digital design. The module Embedded Systems for FPGA exposes students to hardware and software partitioning and codesign for embedded systems, common embedded systems peripherals and embedded systems programming using both high- and low-level languages. Students gain experience in implementing DSP, hardware accelerators, and custom peripherals for FPGA-based embedded systems and programming embedded systems. The knowledge and skills from the above module lead to effective design and implementation of hardware components for digital systems.

The project preparation begins towards the end of the Autumn term when groups are given a Quality Assurance manual to prepare them for effective company policies, procedures and roles for group members, introducing the Quality Assurance processes applied to medium to large projects in industry. In the Summer term, the project process continues with the pre-implementation phase in the Design Exercise module. Students design a custom PCB with the components (FPGA, communication interfaces, displays, memories, etc.) defined in the system specifications. The design is sent off for fabrication and returned by the end of term. Along with the PCB design, the students develop a block-level algorithmic description of the system to be implemented, defining the role of each component within the system and beginning the development of the software components of the system. The PCB is tested by verifying the operation of individual components. The software interface on the host PC is finalised and the board-to-PC communication instantiated. The core of the system, i.e., the implementation of the algorithm in the FPGA circuit, is designed, simulated, realised, and verified. The simulation and debugging techniques acquired in the taught modules are employed to ensure correct operation of the system. The outcome of this final part of the project is the actual realisation of the system implemented on the custom-designed PCB.

v) ... how this programme (as outlined in these PLOs) will develop students' digital literacy skills and how technology-enhanced learning will be used to support active student learning through peer/tutor interaction, collaboration and formative (self) assessment opportunities (reference could be made to such as blogging, flipped classroooms, response 'clickers' in lectures, simulations, etc).

The entire programme is imbued with developing digital literacy. A variety of programming languages are encountered and applied by students (PLOs 1-4) as a key part of the modules. The field of Digital Systems Engineering can only exist with a deep understanding of the design and use of hardware and software systems, and so this is built in deeply to the module and programme structure. Students not only learn how to *use* digital tools, but how to *design and build* them. PLO1 enhances personal research by developing students' skills to independently find, evaluate and use sources. Students also need to develop their personal communication skills (PLO5) and the programme and its assignments provide multiple opportunities for this; from keeping technical logbooks, to portraying information to the public via poster preparation, and by doing public presentations. PLO6 is developed not only in the module assignments (managing themselves, teams and complex projects) which use collaborative tools such as Google Apps, but in the final teamworking project, and by involvement in the Professional Development Framework (see below in 5.c. vi).

vi) ... how this programme (as outlined in these PLOs) will support and enhance the students' employability (for example, opportunities for students to apply their learning in a real world setting)?
The programme's employablity objectives should be informed by the University's Employability Strategy:
http://www.york.ac.uk/about/departments/support-and-admin/careers/staff/

All our MScs programmes incorporate a carefully designed Professional Development Framework. In consultation with our Departmental Advisory Board, with key contributors from Industry, Research and Academia, this ensures that all students gain awareness of the essential skills that employers need and opportunities to develop their personal and team-based effectiveness. This begins with an Induction Week including an introduction to masters-level learning, and student team activities. Throughout the Autumn and Spring Terms students develop their personal effectiveness in a series of workshops (covering such issues as literature, research, referencing, teamwork, leadership, reflective learning, ethics, and business skills). These lead on to Interdisciplinary Masterclasses which cover key research and development cross-curricular topics in emerging technology. In the Summer Term students are prepared for research methodology and digital literacy, and undertake regular developmental training in project management. This all leads to a major group project (60 credit units) which is designed to give research and industry-relevant experience to individuals and teams as a major component of each programme.

viii) ... how learning and teaching on the programme are informed and led by research in the department/ Centre/ University?

York's world-leading Intelligent Systems and Nano-Science Research Group specialises in the application of biological techniques to complex digital systems, and makes full use of the industry-standard FPGA design and development facilities within the Department of Electronic Engineering. Modules are informed by this research and development and are kept up to date with the latest research, equipping them with state-of-the-art knowledge in this rapidly evolving area. Students have multiple opportunities to work with and be guided by staff who are actively working in these developing subject fields.

5.d. Progression

For masters programmes where students do not incrementally 'progress' on the completion of a discrete Postgraduate Certificate and Postgraduate Diploma, please summarise students' progressive development towards the achievement of the PLOs, in terms of the characteristics that you expect students to demonstrate at the end of the set of modules or part thereof. This summary may be particularly helpful to students and the programme team where there is a high proportion of option modules and in circumstances where students registered on a higher award will exit early with a lower one.

Note: it is not expected that a position statement is written for each masters PLO, but this can be done if preferred.

On completion of modules sufficient to obtain a Postgraduate Certificate students will be able to:

If the PG Cert is an exit award only please provide information about how students will have progressed towards the diploma/masters PLOs. Please include detail of the module diet that students will have to have completed to gain this qualification as an exit award.

Students can receive a postgraduate certificate by achieving a minimum of 60 credits in taught modules. This could occur for instance by failing a pass/fail module, or by not being able to progress onto the project for other reasons such as failing the Research Methods or Design Exercise modules. Up to this point in the programme all PLOs are covered, but PLO1 will be lacking the literature review contextualisation, and PLO6 will be under-practiced as the major project is not experienced.

On completion of modules sufficient to obtain a Postgraduate Diploma students will be able to:

If the PG Diploma is an exit award only please provide information about how students will have progressed towards the masters PLOs. Please include detail of the module diet that students will have to have completed to gain this qualification as an exit award.

Students can receive a Diploma by passing everything except the project (due to leaving early or by failing the project). Thus they will have covered the majority of PLOs 1-5. Their completion of PLO6 will be limited compared to a Masters graduate, but it is not entirely missing as they will have still have completed the Research Methods and Design Exercise modules and attended support sessions on Project Management.

6. Reference points and programme regulations

6.a. Relevant Quality Assurance Agency benchmark statement(s) and other relevant external reference points

Please state relevant reference points consulted (e.g. Framework for Higher Education Qualifications, National Occupational Standards, Subject Benchmark Statements or the requirements of PSRBs): See also Taught Postgraduate Modular Scheme: Framework for Programme Design:

Framework for Higher Education Qualifications in England, Wales and Northern Ireland – August 2008 http://www.qaa.ac.uk/Publications/InformationAndGuidance/Documents/FHEQ08.pdf
IET Accreditation – October 2014: http://www.theiet.org/academics/accreditation/policy-guidance/

6.b. University award regulations

The University's award and assessment regulations apply to all programmes: any exceptions that relate to this programme are approved by University Teaching Committee and are recorded at the end of this document.

7. Programme Structure

7.a. Module Structure and Summative Assessment Map
Please complete the summary table below which shows the module structure and the pattern of summative assessment through the programme.

IMPORTANT NOTE:
If the structure of your programme does not fit the usual academic year (for instance students start at the beginning of September or in January) please contact your Academic Quality Team contact in the Academic Support Office for guidance on how to represent the structure in an alternative format.

To clearly present the overall programme structure, include the name and details of each invidual CORE module in the rows below. For OPTION modules, 'Option module' or 'Option from list x' should be used in place of specifically including all named options. If the programme requires students to select option modules from specific lists by term of delivery or subject theme these lists should be provided in the next section (7.b).

From the drop-down select 'S' to indicate the start of the module, 'A' to indicate the timing of each distinct summative assessment point (eg. essay submission/ exam), and 'E' to indicate the end of teaching delivery for the module (if the end of the module coincides with the summative assessment select 'EA'). It is not expected that each summative task will be listed where an overall module might be assessed cumulatively (for example weekly problem sheets).

Summative assessment by exams should normally be scheduled in the spring week 1 and summer Common Assessment period (weeks 5-7). Where the summer CAP is used, a single 'A' can be used within the shaded cells as it is understood that you will not know in which week of the CAP the examination will take place. (NB: An additional resit assessment week is provided in week 10 of the summer term for postgraduate students. See Guide to Assessment, 5.4.a)

Full time structure

Credits	Module		Autumn Term										Spring Term										Summer Term										Summer Vacation												
	Code	Title	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10	11	12	13
20	ELE00089M	Integrated Circuit Design & Simulation		S								E	A																																
20	ELE00067M	Digital Design		S			A					E		A																														
10	ELE00107M	C Programming for MSc		S								E			A																														
10	ELE00013M	Embedded Systems for FPGA												S							A	E	A																						
10	ELE00063M	Systems Programming for Embedded Devices												S								E	A																						
10	ELE00121M	Digital Engineering for MSc												S					A			E	A																						
20	ELE00111M	MSc Personal Effectiveness and Masterclasses		S																		EA																						

10	ELE00122M	Design Exercise																					S	A							E	A													
10	ELE00123M	Research Methods Theory																					S		S	EA																			
60	ELE00048M	MSc Digital Systems Engineering Project																					S										A										EA	A	

Full-time Route: Please indicate when the Progression Board and Final Exam board will be held and when any reassessments will be submitted.
NB: You are required to provide at least three weeks notice to students of the need for them to resubmit any required assessments, in accordance with the Guide to Assessment section 4.9

Progression Board	Week 2 Summer Vacation
Reassessment	Week 7 Summer Vacation
Exam Board	Autumn Term Week 3

Part time structures
Please indicate the modules undertaken in each year of the part-time version of the programme. Please use the text box below should any further explanation be required regarding structure of part-time study routes.

Year 1 (if you offer the programme part-time over either 2 or 3 years, use the toggles to the left to show the hidden rows)

Year 2

Year 3

7.b. Optional module lists

If the programme requires students to select option modules from specific lists these lists should be provided below. If you need more space, use the toggles on the left to reveal ten further hidden rows.

Option List A	Option List B	Option List C	Option List D

7.c. Explanation of the programme and assessment design
The statements should be in a form that can be used for students (such as in a student handbook). It should make clear to students why they are doing the key activities of the programme, in terms of reaching the PLOs.

i) Students' independent study and formative work Please outline how independent study and student work has been designed to support the progressive achievement of the programme learning outcomes (for example, the use of online resources which incorporate formative feedback; opportunities for further learning from work-based placements).

Key texts are given to read, as well as information about, for example, the programming language being taught, or the digital engineering principles being described. As the programme progresses, increasing amounts of the students' time is spent working on more specialised material, culminating in a major project. All modules incorporate a major component of independent study, but the Group Project is the culmination of independent work. The project requires candidates to carry out research and a technical literature review to support high-level and low-level design decisions and for the actual design and implementation; to determine design methodologies, and integrate, test and verification methodologies for both hardware and software; DSP techniques, and their implementation using a suitable combination of hardware and software; the use of industry standard tool chains; and application notes, datasheets, reference manuals, among other textbook material. Throughout this whole process the Professional Development Framework provides an opportunity to work with all Masters students in the Department to develop key skills and competencies that have been developed with our consultations with industry.

ii) Contact with staff
Please explain how the programme's design maximises the value of students' contact time with staff (which may be face-to-face, virtual, synchronous or asynchronous), including through the use of technology-enhanced learning. For example, giving students resources for their independent study which then enables a class to be more interactive with a greater impact on learning.

In the first term of the programme, students have access to intensive periods of study by staff in lectures, labs, tutorials and supervisions. Lab assistants are also available to help with practical work. On-line materials are provided in advance of lectures, laboratories and workshops in order to facilitate and make the most effective use of contact time, through effective preparation. Students have access at any time to a personal supervisor who is there to guide them through the process and help them reflect on their learning and progress. In addition to scheduled meetings, students are encouraged to contact their personal supervisors and module coordinators on a needs basis. All modules have self-study materials available such as lecture notes, lab-scripts etc, which students are expected to read, and these can then be discussed with staff during taught sessions. Contact time changes during the Summer period to a more supervisory role, where students have access to two project supervisors (who are not necessarily their academic supervisor) and here the focus is on supporting, developing and progressing the final project. Meetings are typically held on a weekly basis, with individual students and whole project groups encouraged to contact their lead project supervisor as technical queries arise.

iii) Summative Assessment
Please outline how summative assessment within and across modules has been designed to support and evidence the progressive achievement of the programme learning outcomes. (For example, the use of different assessment methods at the 'introduction' stage compared to those used to evaluate deeper learning through the application of skills and knowledge later in the programme).

This programme has a mix of summative assessment styles. Theoretical modules are usually assessed by closed-book examination. Several assignments are designed to be more than just a test, but to provide a challenging experience for personal work. Scenarios are given for each such assignment which reflect the range of real-world applications that the students may encounter in this topic area. Early stage assessment is more restricted to testing the knowledge and understanding of fundamental theory and its application to practical problems. Beyond the Autumn term, assessments include parts which require the students to apply their knowledge to solve particular problems. In modules during the later stages of the degree programme, notably the group project, every student is required to be creative and develop their own designs and solutions to challenging problems in Digital Systems Engineering. Thus later assignments, including the final project, tend to cover most PLOs as they require the application of knowledge (PLO1), the analysis and design of a problem (PLOs 2 & 3), the practical building and development of a technical solution (PLO4), managed in a creative and effective way (PLO6) and described effectively to others (PLO5). As the programme progresses, the assignments incorporate a greater degree of student innovation and independence, culminating in a final creative and technical project.

8. Additional information

8.a. Continuing Professional Development
Will any of the programme's modules be available on a free-standing basis?

Please Select Y/N:	No	

8.b. Transfers out of or into the programme

i) Transfers into the programme will be possible? (please select Y/N)	No	
ii) Transfers out of the programme will be possible? (please select Y/N)	No	

11. Exceptions to University Award Regulations approved by University Teaching Committee

Exception Please detail any exceptions to University Award Regulations approved by UTC	**Date approved**
N/A	N/A

Quality and Standards

The University has a framework in place to ensure that the standards of its programmes are maintained, and the quality of the learning experience is enhanced.

Quality assurance and enhancement processes include:

· the academic oversight of programmes within departments by a Board of Studies, which includes student representation
· the oversight of programmes by external examiners, who ensure that standards at the University of York are comparable with those elsewhere in the sector
· annual monitoring and periodic review of programmes
· the acquisition of feedback from students by departments, and via the Postgraduate Taught Experience Survey (PTES).

More information can be obtained from the Academic Support Office:

Date on which this programme information was updated:
26 Sept 2019
Departmental web page:
https://www.york.ac.uk/electronic-engineering/postgraduate/taught_masters_degrees/msc_dse__
Please note: The information above provides a concise summary of the main features of the programme and the learning outcomes that a typical student might reasonably be expected to achieve and demonstrate if they take full advantage of the learning opportunities that are provided. Detailed information on the learning outcomes, content, delivery and assessment of modules can be found in the module descriptions. The University reserves the right to modify this overview in unforeseen circumstances, or where the process of academic development, based on feedback from staff, students, external examiners or professional bodies, requires a change to be made. Students will be notified of any substantive changes at the first available opportunity.

Template Last Updated 11/01/2017 by Adrian Lee

Overview of modules by stage

Notes:

[1] The credit level is an indication of the module's relative intellectual demand, complexity and depth of learning and of learner autonomy (Level 4/Certificate, Level 5/Intermediate, Level 6/Honours, Level 7/Masters).....

[2] The credit value gives the notional workload for the module, where 1 credit corresponds to a notional workload of 10 hours (including contact hours, private study and assessment)...

[3] Special assessment rules (requiring University Teaching Committee approval); P/F – the module marked on a pass/ fail basis (NB pass/ fail modules cannot be compensated); NC – the module cannot be compensated; NR – there is no reassessment opportunity for this module. It must be passed at the first attempt

[4] Independent Study Modules (ISMs) are assessed by a dissertation or substantial project report. They cannot be compensated (NC) and are subject to reassessment rules which differ from 'taught modules'. Integrated Masters programmes may designate a project in the final stage as an ISM which is then subject to the assessment rules as set out in the postgraduate programmes section of the Guide to Assessment.

Core & option module table (add additional rows as required)

Core/ Option	New/ substantially revised module – Yes/ No	Module title	Module code	Credit level[1]	Credit value[2]	Prerequisites, Corequisites, Prohibited combinations (name of modules(s))	Assessment rules[3],[4]	Timing of module (eg. AuT – Autumn, SpT – Spring, SuT – Summer Term, Year long)	Format, contribution to module mark and timing of summative assessment (eg. essay, 50%, AuT wk10, exam and 50%, SpT wk1)
Core	No	Integrated Circuit Design & Simulation	ELE00089M	7/M	20			AuT	Closed exam, 100%, SpT wk1
Core	No	Digital Design	ELE00067M	7/M	20			AuT	Lab Reports 30%, AuT wk8, Homework 40% wk1, SpT, Final Project wk3, SpT
Core	No	C Programming for MSc	ELE00107M	7/M	10			AuT	C Program & Report, 100%, SpT wk 3
Core	No	Embedded Systems for FPGA	ELE00013M	7/M	10			SpT	Oral Presentation, 30%, SpT wk9, Report, 70%, SuT wk 1
Core	No	Systems Programming for Embedded Devices	ELE00063M	7/M	10			SpT	Design Report, 100%, SuT wk 1
Core	No	Digital Engineering for MSc	ELE00121M	7/M	10	Digital Design - ELE00067M		SpT	Lab Reports 1, 50%, SpT wk 7, Lab Reports 2, 50%, SuT wk 1
Core	Yes	MSc Personal Effectiveness and Masterclasses	ELE00111M	7/M	20			AuT, SpT	Portfolio of work, 100%, SpT wk10

Core	Yes	Design Exercise	ELE00122M	7/M	10			SuT	In class test, 20%, SuT wk 2, Group Presentation, 80%, SuT wk 10
Core	Yes	Research Methods Theory	ELE00123M	7/M	10			SuT, SuV	Individual Report, 100%, SuT wk4
Core	No	MSc Digital Systems Engineering Project	ELE00048M	7/M	60		ISM	SuT, SuV	Initial Report 20%, SuV wk 1, Final report, 50%, SuV wk 11, Presentation and Demo , 10%, SuV wk 12, Performance Review 10%, SuV wk 12, Viva 10%, SuV wk 12